PDHonline Course E277 (4 PDH)

Operational Amplifier Stability and Common-Mode Noise Rejection

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OFFSET CONSIDERATIONS

The practical Op Amp, unlike the hypothetical ideal version, has some dc output voltage we are calling *output offset* voltage, even though both of its inputs are grounded. Such an output offset is an error voltage and is generally undesirable. The causes and cures of output offset voltages are the subjects of this chapter. Here we will become familiar with parameters that enable us to predict the maximum output offset voltage that a given Op Amp circuit can have. On the foundation laid in this chapter, we will build an understanding of why, and an ability to predict how much, a given Op Amp's output voltage tends to drift with power supply and temperature changes, which are important subjects discussed later.

4.1 INPUT OFFSET VOLTAGE V_{io}

The input offset voltage V_{io} is defined as the amount of voltage required across an Op amp's inputs 1 and 2 to force the output voltage to 0 V. In a previous chapter we learned that ideally, when the differential input voltage $V_{id} = 0$ V, as in Fig. 4-1, the output offset V_{oo} is 0 V too. In the practical case, however, V_{oo} voltage will always be present. This is caused by imbalances within the Op amp's circuitry. They occur because the transistors of the input differential stage within the Op Amp usually admit slightly different collector currents even though both bases are at the same potential. This causes a differential output voltage from the first stage, which is amplified and possibly aggravated by more imbalances in the following stages. The combined result of these imbalances is the output offset voltage V_{oo}. If small dc voltage of proper polarity is applied to inputs 1 and 2, it will decrease the

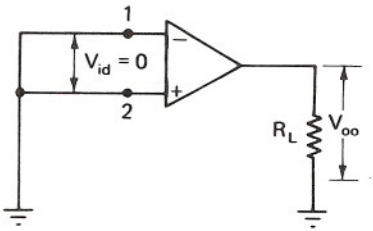

Figure 4-1 Ideally, $V_{oo} = 0$.

output voltage. The amount of differential input voltage, of the correct polarity, required to reduce the output to 0 V is the input offset voltage V_{io}. When the output is forced to 0 V by the proper amount and polarity of input voltage, the circuit is said to be *nulled* or *balanced*. The polarity of the required input offset voltage V_{io} at input 1 with respect to input 2 might be positive as often as negative. This means that the output offset voltage, before nulling, can be positive or negative with respect to ground.

A typical nulling circuit of inverting-mode amplifiers is shown in Fig. 4-2. An equivalent for noninverting amplifiers is shown in Fig. 4-3. In each of these circuits, the potentiometer POT can be adjusted to provide the value

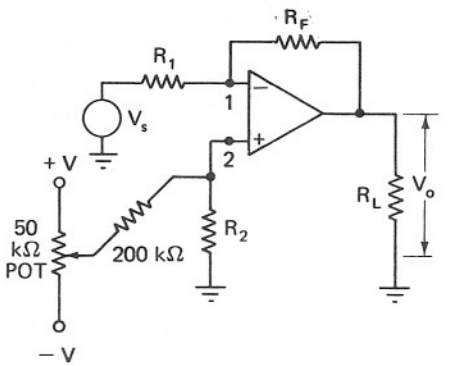

Figure 4-2 Typical null balancing circuit in inverting amplifiers.

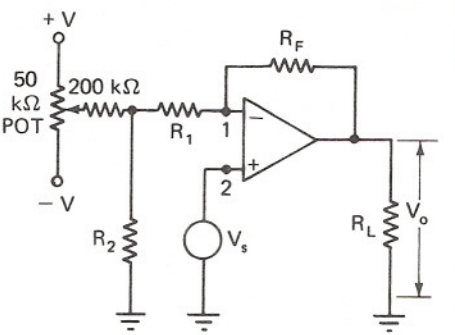

Figure 4-3 Typical null balancing circuit in noninverting amplifiers.

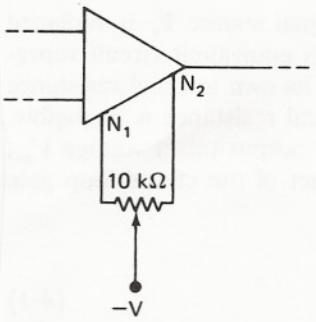

Figure 4-4 Available null adjustment for a 741 Op Amp.

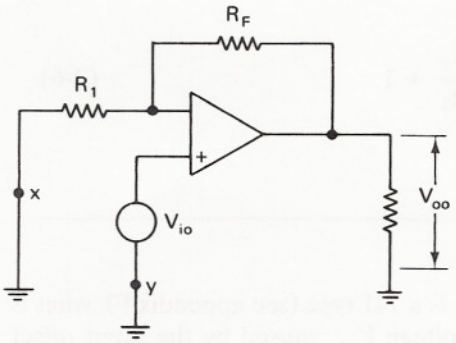

Figure 4-5 Equivalent circuit of either the inverting or the noninverting amplifier.

and polarity of dc input voltage required to null the output to 0 V. As shown, the ends of the POT are connected to the positive and negative rails. With some Op Amps, such as types 748, 777, 201, 741,* etc. (see Appendix E), *offset adjust* pins are provided. A POT can be placed across the OFFSET NULL pins of a 741, as shown in Fig. 4-4. Adjustment of this POT will null the output if the closed-loop gain A_v is not too large.

If an Op Amp circuit is not nulled, more or less output offset voltage V_{oo} exists, depending on its specified input offset voltage V_{io}, closed-loop gain A_v, and other factors that are discussed in the following sections.

To predict how much output offset V_{oo} a given Op Amp circuit will have, "caused" by its input offset voltage V_{io}, a noninverting amplifier model can be used—see Fig. 4-5. In other words, if $V_B = 0$ V with either the inverting or noninverting amplifier circuit, its model is the circuit of Fig. 4-5. As shown in this figure, the Op Amp's specified input offset voltage V_{io} is equivalent to a dc signal source working into a noninverting type amplifier. If this model in

Fig. 4-5 represents an inverting amplifier, the signal source V_s is replaced with its own internal resistance at point x. If this equivalent circuit represents a noninverting amplifier, V_s is replaced with its own internal resistance at point y. A short circuit replaces V_s if its internal resistance is negligible. According to Fig. 4-5 then, we can show that the output offset voltage V_{oo}, "caused by" the input offset voltage, is the product of the closed-loop gain and the specified V_{io}:

$$\boxed{V_{oo} = A_v V_{io},} \tag{4-1}$$

where

$$A_v \cong \frac{R_F}{R_1} + 1. \tag{3-6}$$

Example 4-1

If the Op Amp in the circuit of Fig. 4-6 is a 741 type (see appendix F), what is the *maximum* possible output offset voltage V_{oo}, caused by the input offset voltage V_{io} before any attempt is made to null the circuit with the 10-kΩ POT?

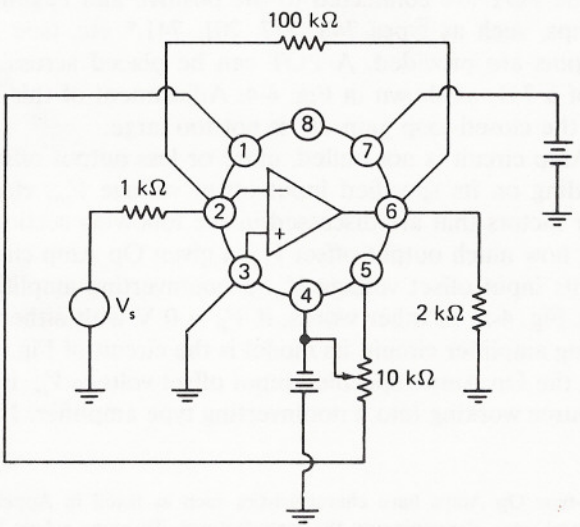

Figure 4-6 741 Op Amp with null adjust POT.

Answer. According to the specifications of the 741, its maximum $V_{io} = 6$ mV. Since the input resistance $R_1 = 1$ kΩ, assuming that the internal resistance of V_s is negligible and since the feedback resistance $R_F = 100$ kΩ, the input offset voltage is multiplied by

$$A_v \cong \frac{R_F}{R_1} + 1 = \frac{100\ \text{k}\Omega}{1\ \text{k}\Omega} + 1 = 101.$$

Therefore, before the circuit is nulled, we might have an output offset as large as

$$V_{oo} = A_v V_{io} \cong 101(6\ \text{mV}) = 606\ \text{mV, or about } 0.6\ \text{V}.$$

This means that the output voltage with respect to ground can be either a positive or a negative 0.6 V even though the input signal $V_s = 0$ V.

4.2 INPUT BIAS CURRENT I_B

Most types of IC Op Amps have two transistors in the first (input) differential stage. Transistors, being current-operated devices, require some base bias currents. Therefore, small dc bias currents flow in the input leads of the typical Op Amp as shown in Fig. 4-7. An input bias current I_B is usually specified on the Op Amp specification sheets as shown in the Appendices. It is defined as the average of the two base bias currents; that is,

$$\boxed{I_B = \frac{I_{B_1} + I_{B_2}}{2}.} \tag{4-2}$$

These base bias currents, I_{B_1} and I_{B_2} are *about* equal to each other, and therefore the specified input bias current I_B is *about* equal to either one of them; that is,

$$\boxed{I_B \cong I_{B_1} \cong I_{B_2}.} \tag{4-3}$$

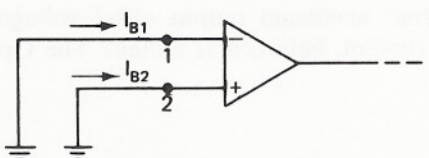

Figure 4-7 Base bias currents flow into the Op Amp and return to ground through the power supplies.

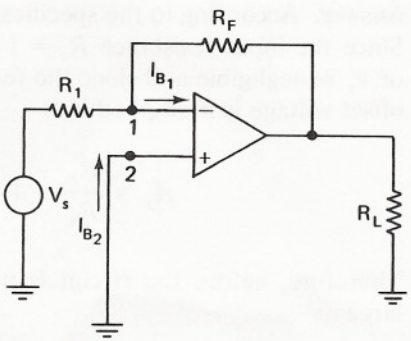

Figure 4-8 Current I_{B_1} sees some resistance on its way to ground, whereas I_{B_2} sees a short.

Depending on the type of Op Amp, the value of input bias current is usually small, generally in the range from a few to a few hundred nanoamperes in general-purpose, economical Op Amps. Though this seems insignificant, it can be a problem in circuits using relatively large feedback resistors, as we will see.

A difficulty that the base bias currents might cause can be seen if we analyze their effect on a typical amplifier such as in Fig. 4-8. Note that I_{B_2} flows out of ground directly into input 2. (See Fig. 1-8 for the current paths of a typical differential input stage.) Therefore, input 2 is 0 V with respect to ground. On the other hand, base bias current I_{B_1} sees resistance on its way to input 1, that is, the parallel paths containing R_1 and R_F have a total effective resistance as seen by the base bias current I_{B_1}. The flow of I_{B_1} through this effective resistance causes a dc voltage to appear at input 1. With a dc voltage to ground at input 1 while input 2 is 0 V to ground, a dc differential input voltage V_{id} appears *across* these inputs. This dc input amplified by the closed-loop gain causes an output offset voltage V_{oo}. The amount of output offset voltage V_{oo}, caused by the base bias current I_{B_1}, can be approximated with the equation

$$\boxed{V_{oo} \cong R_F I_B,} \qquad (4\text{-}4)^*$$

where $I_B \cong I_{B_1}$, and is usually specified by the manufacturer.

Example 4-2

Referring to the circuit in Fig. 4-6, what maximum output offset voltage might it have, caused by the base bias current, before it is nulled? The Op Amp is a type 741.

*See Appendix G for the derivation.

Answer. According to the 741's specification sheets (Appendix F), the maximum input bias current $I_B = 500$ nA. Since $R_F = 100$ kΩ, the base bias current could cause an output offset as large as

$$V_{oo} \cong R_F I_B = 100\ \text{k}\Omega(500\ \text{nA}) = 50\ \text{mV}. \qquad (4\text{-}4)$$

We should note in these last two examples that the output offset caused by the input offset voltage V_{io} is about 10 times larger than the output offset caused by the input bias current I_B. In this case then, the input offset voltage V_{io} is potentially the greater problem. However, according to Eq. (4-4), we can see that the output offset V_{oo} caused by the bias current I_B is larger, and therefore potentially more troublesome, with larger values of feedback resistance R_F.

Example 4-3

Referring again to the circuit of Fig. 4-6, suppose that we replace the 1-kΩ input resistor with 100 kΩ and the 100-kΩ feedback resistor with 10 MΩ:

(a) How does this affect the closed-loop gain A_{v} of this circuit compared to what it was originally? Before any attempt is made to null this circuit, find

(b) Its maximum output offset caused by the input offset voltage V_{io}, and

(c) The maximum output offset caused by the input bias current I_B. The Op Amp is still a type 741.

Answers

(a) The closed-loop gain A_{v} is unchanged; that is, this circuit's gain is very nearly equal to the ratio R_F/R_1, which was not changed.

(b) With no change in the closed-loop gain, the output offset caused by the input offset voltage does not change [see Eq. (4-1)].

(c) The output offset caused by input bias current I_B is larger with circuits using larger feedback resistors. according to Eq. (4-4). Thus in this case

$$V_{oo} \cong R_F I_B = 10\ \text{M}\Omega(500\ \text{nA}) = 5\ \text{V}.$$

This is a relatively large output offset. And approaches the positive rail of some Op Amp circuits. This example presents a good case for the use of small feedback resistors.

The effect of the input bias current I_B on the output offset voltage can be minimized if a resistor R_2 is added in series with the noninverting input as

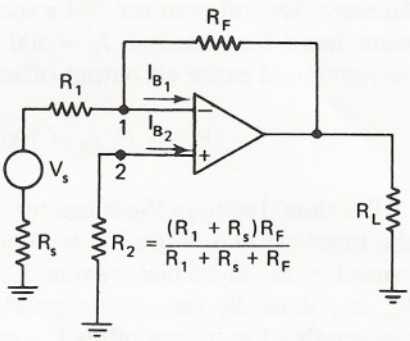

Figure 4-9 Resistor R_2 in series with the noninverting input reduces the output offset voltage caused by the input bias current I_B.

shown in Fig. 4-9. By selecting the proper value of R_2, we can make the resistance seen by the base bias current I_{B_2} equal to the resistance seen by the base bias current I_{B_1}. This will raise input 2 to the dc voltage at input 1. In other words, if the currents I_{B_1} and I_{B_2} are equal, and the resistances seen by these currents are equal, the voltages to ground at inputs 1 and 2 are equal. This means that there will be no dc differential input voltage V_{id} to cause an output offset V_{oo}. The value of R_2 needed to eliminate or reduce the dc differential input voltage V_{id} and the resulting output offset V_{oo} is easily found.

Note in Fig. 4-9 that current I_{B_1} sees two parallel paths, one containing R_1 and R_s in series and the other containing R_F. Thus when $V_o \cong 0$ V, current I_{B_1} sees a resistance $R_1 + R_s$ in parallel with the feedback resistor R_F. Since current I_{B_2} is to see a resistance R_2 that is equal to the total resistance seen by I_{B_1}, we can show that

$$R_2 = \frac{(R_1 + R_s)R_F}{R_1 + R_s + R_F}. \tag{4-5a}$$

If the internal resistance of the signal source is zero, then

$$R_2 = \frac{R_1 R_F}{R_1 + R_F}. \tag{4-5b}$$

Example 4-4

Referring to the circuit in Fig. 4-6, what value of resistance can we use in series with the noninverting input (pin 3) to reduce or eliminate the output offset voltage caused by the input bias current? Assume that the internal resistance of the signal source V_s is negligible.

Answer. Since the input resistor $R_1 = 1\ \text{k}\Omega$, the feedback resistor $R_F = 100\ \text{k}\Omega$, and the signal source's resistance $R_s = 0\ \Omega$, we can use

$$R_2 = \frac{(1\ \text{k}\Omega + 0)100\ \text{k}\Omega}{1\ \text{k}\Omega + 0 + 100\ \text{k}\Omega} = 990\ \Omega.$$

4.3 INPUT OFFSET CURRENT I_{io}

In the previous section we learned that a resistor R_2 placed in series with the noninverting input 2 reduces the output offset caused by the input bias current. However, Eq. (4-5) for finding the necessary value of R_2 was derived assuming that the base bias currents I_{B_1} and I_{B_2} are equal. In practice, due to imbalances within the Op Amp's circuitry, these currents are at best only approximately equal, as indicated in Eq. (4-3). The input offset current I_{io}, usually specified by the manufacturer, is a parameter that indicates how far from being equal the currents I_{B_1} and I_{B_2} can be. In fact, the input offset current is defined as the difference in the two base bias currents; that is,

$$\boxed{I_{io} = |I_{B_1} - I_{B_2}|.} \tag{4-6}$$

When given the value of input offset current I_{io}, we can predict how much output offset voltage a circuit like that in Fig. 4-9 might have, caused by the existence of base bias currents. Due to inequalities of the currents I_{B_1} and I_{B_2}, the voltages with respect to ground at inputs 1 and 2 will be unequal, even though a properly chosen value of R_2 is used. This causes a dc differential input voltage V_{id}, which in turn causes an output offset voltage V_{oo}. In other words, the amount of dc differential input voltage and the amount of resulting output offset depend on the amount of difference in the base bias currents I_{B_1} and I_{B_2}, which is the input offset current I_{io}. More specifically, the amount of output offset voltage V_{oo} in a circuit like that in Fig. 4-9, caused by the input offset current I_{io}, can be closely approximated with the equation

$$\boxed{V_{oo} \cong R_F I_{io}} \tag{4-7}^*$$

if the value of R_2 is determined with Eq. (4-5).

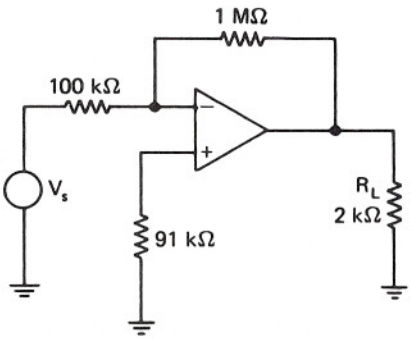

Figure 4-10 Circuit for Example 4-5.

Example 4-5

Referring to the circuit in Fig. 4-10, find the maximum output offset caused by the input offset current I_{io}. The Op Amp is a type 741, and the internal resistance of the signal source V_s is negligible.

Answer. The 741's maximum input offset current $I_{io} = 200$ nA as indicated on its specification sheet. Since the value of R_2 satisfies Eq. (4-5), we can closely estimate the output offset caused by I_{io} with Eq. (4-7). In this case

$$V_{oo} \cong R_F I_{io} = 1\ \text{M}\Omega(200\ \text{nA}) = 200\ \text{mV}.$$

This shows that we might have an output offset due to unequal base bias currents even though a properly chosen resistor R_2 is placed between the noninverting input and ground. If R_2 is not used, however, the output offset caused by input currents is considerably larger and therefore potentially a greater problem.

Example 4-6

Referring again to the circuit in Fig. 4-10, find the maximum output offset caused by the input currents if R_2 is removed and, instead, the noninverting input is connected directly to ground. As before, the Op Amp is a type 741.

Answers

$$V_{oo} \cong R_F I_B = 1\ \text{M}\Omega(500\ \text{nA}) = 500\ \text{mV}.$$

It is interesting to note that the output offset can be more than doubled if the resistor R_2 is not used. R_2 may or may not be necessary, depending on how important it is to have little or no output offset. The required stability of the output voltage with temperature changes must be considered too, as we

will see in a later chapter. Some types of IC Op Amps are made with FETs or high-beta transistors* in the input differential stage. These have dc input currents on the order of just a few nanoamperes. Some *hybrid* models of Op Amps, which contain discrete and integrated circuits, have input bias currents in the order of 0.01 pA or less. Of course, such a small dc input bias current reduces the current-generated output offset voltage to insignificance. As we will see in applications later, an extremely small input bias current is desirable, and in fact necessary, in long-term integrating and sample-and-hold circuits.

4.4 COMBINED EFFECTS OF V_{io} AND I_{io}

In a circuit such as that in Fig. 4-9, the input offset voltage V_{io} can cause either a positive or a negative output offset voltage V_{oo} [see Eq. (4-1)]. Likewise, the input offset current I_{io} can cause either a positive or a negative output offset voltage V_{oo} [see Eq. (4-7)]. The effects of input offset voltage V_{io} and input offset current I_{io} might buck and cancel each other, resulting in little output offset. On the other hand, they might be additive, causing an output offset voltage V_{oo} that is the sum of the output offsets caused by V_{io} and I_{io} working independently. Thus the total output offset voltage in the circuit of Fig. 4-9 can be as large as

$$\boxed{V_{oo} \cong A_v V_{io} + R_F I_{io}} \tag{4-8a}$$

if the value of R_2 satisfies Eq. (4-5). This equation is sometimes shown in other equivalent forms, such as

$$\boxed{V_{oo} \cong [V_{io} + R_2 I_{io}]\left(\frac{R_F}{R_1} + 1\right)} \tag{4-8b}$$

or

$$\boxed{V_{oo} \cong \left[V_{io} + R_2(I_{B_1} - I_{B_2})\right]\left(\frac{R_F}{R_1} + 1\right)} \tag{4-8c}$$

Example 4-7

Considering the effects of both V_{io} and I_{io}, what is the maximum output offset voltage V_{oo} of the circuit in Fig. 4-10 if the Op Amp is a type 741?

Answer. Arbitrarily selecting Eq. (4-8b), we can show that the maximum output offset voltage is

$$V_{oo} \cong [6\ \text{mV} + 91\ \text{k}\Omega(200\ \text{nA})]\left(\frac{1000 + 100}{100}\right) = 266\ \text{mV}.$$