PDHonline Course E277 (4 PDH)

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Operational Amplifier Stability and Common-Mode Noise Rejection

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COMMON-MODE VOLTAGES
AND DIFFERENTIAL AMPLIFIERS

Industrial and commercial environments are electrically noisy. Lighting fixtures, motors, relays, and switches, to name just a few, emit time-varying electric and magnetic fields. These fields induce electrical noise into nearby conductors. Noise voltages (V_n) induced into conductors at inputs of amplifiers are amplified along with the signals (V_s) that are intended to be amplified. Thus the amplitudes of both the induced noise V_n and signal V_s are increased together. In many amplifier applications, the leads and interconnections can be kept short and the amplitude of the induced noise, relative to the signal, is small and of no consequence. In applications that require that signals be transported over distances, the induced noise can be very troublesome. For example, remote sensors monitoring temperatures, pressures, tensile stress, etc. are commonly used in industrial and medical equipment. In such applications the induced noise voltages are often larger than the signals that we are trying to amplify. By use of amplifiers with differential inputs, we can make induced noise voltages *common mode*, and as you will see, this will greatly reduce their amplitudes compared to the signals.

A voltage at both inputs of an Op Amp, as shown in Fig. 5-1, is a *common-mode* voltage V_{cm}. A common-mode voltage V_{cm} can be dc, ac, or a combination (superposition) of dc and ac. When Op Amps work in time-varying magnetic and electric fields, noise voltages are induced into both input leads. In such cases, dc and ac common-mode voltages V_{cm} can exist simultaneously at an Op Amp's inputs. The induced ac voltage includes 60 Hz from nearby electrical power equipment and include higher frequencies or even irregular transients. In any case, it is undesired and considered as *noise* in the system.
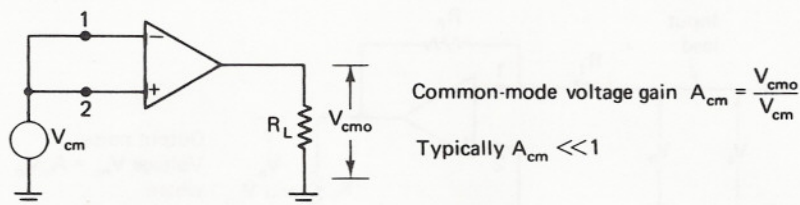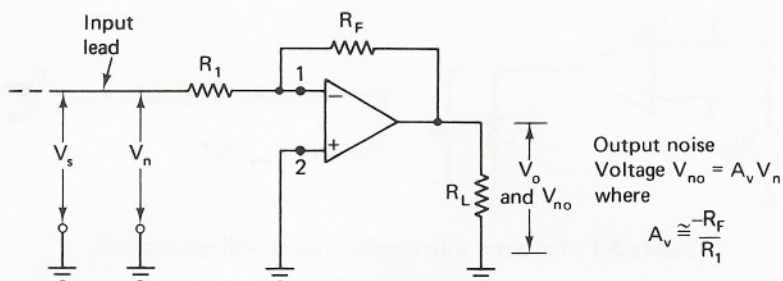
Figure 5-1   Op Amp with common-mode voltage applied.

Amplifiers with differential inputs (e.g., Op Amps) have more or less ability to reject common-mode voltages. This means that, although fairly large common-mode voltages might exist at an Op Amp's differential inputs, these voltages can be reduced to very small and often insignificant amplitudes at the output. In this chapter we will become familiar with manufacturers' specifications that will enable us to predict how well a given Op Amp will reject (not pass) common-mode voltages. We will also see applications in which the Op Amp's ability to reject common-mode voltages is useful.
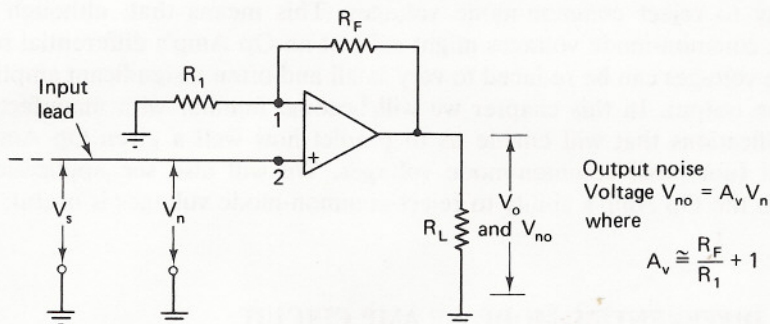
5.1   DIFFERENTIAL-MODE OP AMP CIRCUIT

To appreciate fully how a properly wired Op Amp circuit is able to reject undesirable common-mode voltages, we should first look at the familiar circuits that have induced noise at their inputs. For example, for both circuits shown in Fig. 5-2, voltage V_s is the desired signal to be amplified. If the input lead has any appreciable length, and if varying fields are present, noise voltage V_n will be induced into it as shown. In both of these circuits, the Op Amp cannot distinguish noise V_n from desired signal V_s; both are amplified and appear at the outputs. Thus if the closed-loop gain A_v of each of these circuits is 100, the output noise voltage V_{no} and output signal voltage V_o are 100 times larger than their respective inputs.
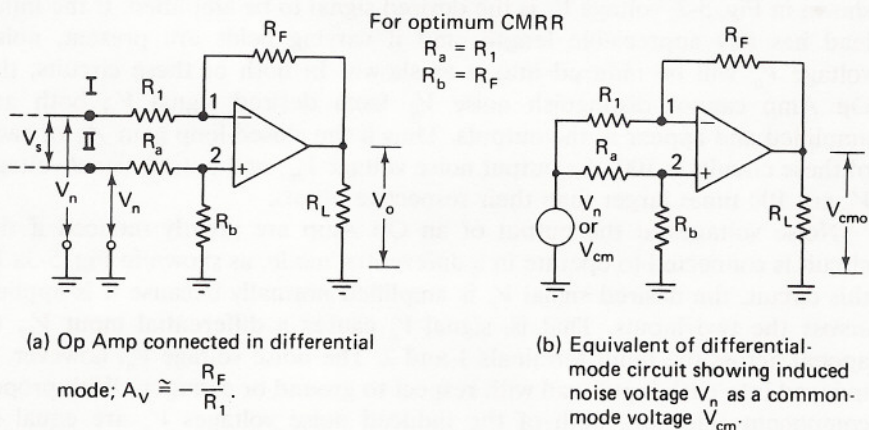
Noise voltages at the output of an Op Amp are greatly reduced if the circuit is connected to operate in a differential mode, as shown in Fig. 5-3a In this circuit, the desired signal V_s is amplified normally because it is applied *across* the two inputs. That is, signal V_s causes a differential input V_{id} to appear across the input terminals 1 and 2. The noise voltage V_n, however, is induced into each input lead with respect to ground or common. With proper component selection, both of the induced noise voltages V_n are equal in amplitude and phase and therefore are common-mode voltages, as shown in Fig. 5-3b. Thus if the noise voltage to ground at input 1 is the same as the noise voltage to ground at input 2, the differential noise voltage across input terminals 1 and 2 is zero. Since ideally an Op Amp amplifies only differential input voltages no noise voltage should appear at the output. However, due to

(a) Inverting-mode amplifier

Output noise Voltage $V_{no} = A_v V_n$ where

$$A_v \cong \frac{-R_F}{R_1}$$

(b) Noninverting-mode amplifier

Output noise Voltage $V_{no} = A_v V_n$ where

$$A_v \cong \frac{R_F}{R_1} + 1$$

Figure 5-2   Inverting-mode and noninverting-mode circuits amplify induced noise.

For optimum CMRR
$R_a = R_1$
$R_b = R_F$

(a) Op Amp connected in differential
mode; $A_V \cong - \dfrac{R_F}{R_1}$.

(b) Equivalent of differential-mode circuit showing induced noise voltage V_n as a common-mode voltage V_{cm}.

Figure 5-3   (a) Op Amp connected in differential mode; $A_V \cong -R_F/R_1$. (b) Equivalent of differential-mode circuit showing induced noise voltage V_n as a common-mode voltage V_{cm}.

inherent electrical characteristics of an Op Amp—such as internal capacitances—some common-mode signals will get through to the load R_L. The ratio of the output common-mode voltage V_{cmo} to the input common-mode voltage V_{cm} is called the common-mode gain A_{cm}; that is,

$$A_{cm} = \frac{V_{cmo}}{V_{cm}}. \tag{5-1}$$

Ideally, this gain A_{cm} is zero. In practice, it is finite but usually much smaller than 1.

5.2   COMMON-MODE REJECTION RATIO, CMRR

Op Amp manufacturers do not list a common-mode gain factor. Instead, they list a *common-mode rejection ratio*, CMRR. The CMRR is defined in several essentially equivalent ways by the various manufacturers. It can be defined as the ratio of the change in the input common-mode voltage ΔV_{cm} to the resulting change in input offset voltage ΔV_{io}. Thus

$$CMRR = \frac{\Delta V_{cm}}{\Delta V_{io}}. \tag{5-2}$$

It also is shown to be equal to the ratio of the closed-loop gain A_v to the common-mode gain A_{cm}; that is,

$$CMRR = \frac{A_v}{A_{cm}}. \tag{5-3}$$

Generally, larger values of CMRR mean better rejection of common-mode signals and are therefore more desirable in applications where induced noise is a problem. Later, we will see that the CMRR of an Op Amp tends to decrease with higher common-mode frequencies.
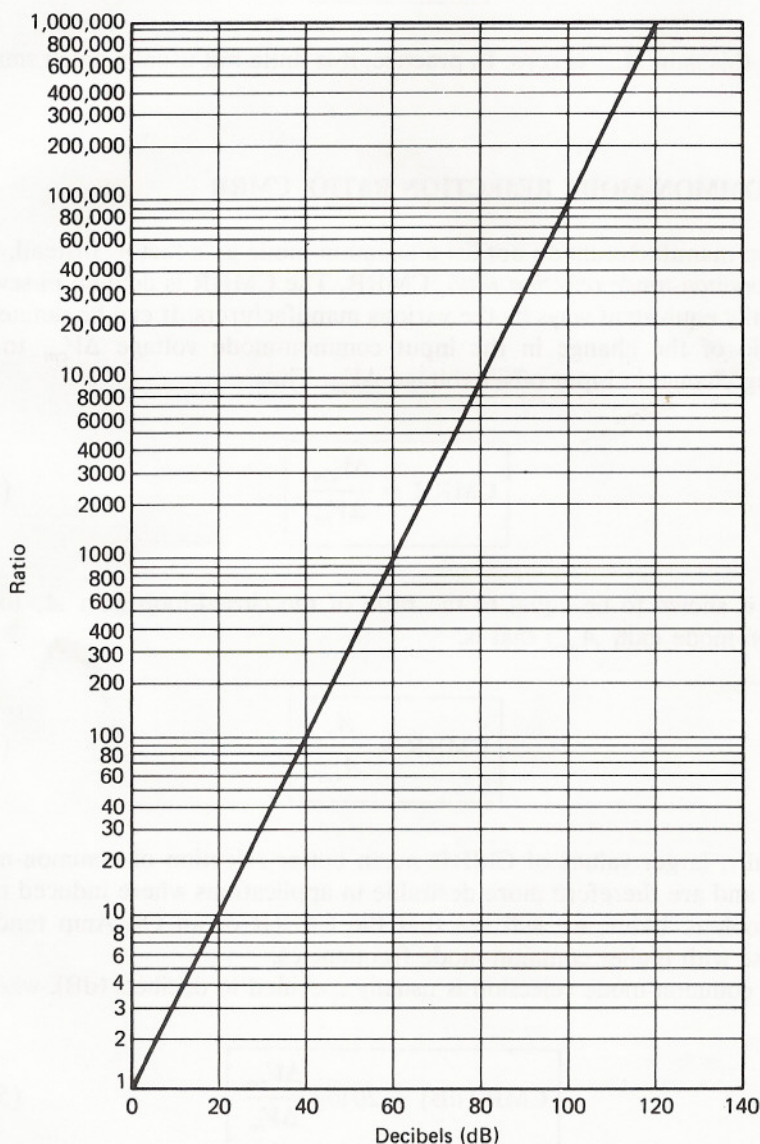
The common-mode rejection is usually specified in decibels (dB), where

$$CMR \ (dB) = 20 \log \frac{\Delta V_{cm}}{\Delta V_{io}} \tag{5-4a}$$

or

$$\text{CMR (dB)} = 20 \log \frac{A_v}{A_{cm}} = 20 \log \text{CMRR}. \qquad (5\text{-}4b)$$

A chart for converting common-mode rejection from a ratio to decibels, or vice versa, is given in Fig. 5-4.

Figure 5-4   Chart for converting voltages ratios to decibels and vice versa.

Equation (5-3) shows that the common-mode voltage gain A_{cm} of a differential-mode Op Amp circuit is a function of its closed-loop gain and the Op Amp's specified CMRR. Rearranging Eq. (5-3), we can show that

$$A_{cm} = \frac{A_v}{\text{CMRR}}.$$

(5-3)

The equivalent of this in decibels can be shown as

$$\boxed{20 \log A_{cm} = 20 \log A_v - 20 \log \text{CMRR}}$$

(5-5a)

or as

$$\boxed{A_{cm}\,(\text{dB}) = A_v\,(\text{dB}) - \text{CMR}\,(\text{dB}).}$$

(5-5b)

Since the closed-loop gain A_v is usually much smaller than the CMRR, the common-mode gain A_{cm} in Eq. (5-3) is much smaller than 1. Therefore, in either version of Eq. (5-5) then, the common-mode gain in decibels is negative.

Some manufacturers define CMRR as the reciprocal of the right side of Eq. (5-2). This implies that the CMRR in decibels is a negative value. If we assume that the specified value of CMR (dB) is positive, then we subtract it from A_v (dB) to obtain the value of A_{cm} (dB), as shown in Eq. (5-5b). If we assume that CMR (dB) is negative, then we add it to A_v (dB) to get A_{cm} (dB). In either case, we solve for the *difference* in the values on the right side of Eq. (5-5) to determine A_{cm} (dB).

The signal voltage gain V_o/V_s of the differential circuit in Fig. 5-3a is determined with Eq. (3-4); that is,

$$|A_v| = \frac{V_o}{V_s} \cong \frac{R_F}{R_1}.$$

(3-4)

Whether this gain is inverting or noninverting is not predictable when calculating the common-mode gain A_{cm}. From the signal's point of view, however, this gain is inverting if we reference signal V_s at input I with respect to input II. If V_s is referenced at input II with respect to input I, this gain A_v is noninverting.

Note in Fig. 5-3a that the resistors R_a and R_b are equal to R_1 and R_F, respectively. Also, the resistances to ground looking back toward the source of V_s from inputs I and II must be equal, and likewise the lead lengths are equal. These design criteria establish conditions that make the noise voltages at these two inputs as equal as possible, that is, common mode. The resistors R_a and R_b also serve the same function as does R_2 in Fig. 4-9. These reduce the output offset V_{oo} caused by bias current I_B.

Example 5-1

Referring to the circuit in Fig. 5-3a, if $R_1 = R_a = 1 \text{ k}\Omega$, $R_F = R_b = 10 \text{ k}\Omega$, $V_s = 10 \text{ mV}$ at 1000 Hz, and $V_n = 10 \text{ mV}$ at 60 Hz, what are the amplitudes of the 1000-Hz signal and the 60-Hz noise at the load R_L? The Op Amp's CMR (dB) = 80 dB.

Answer. This circuit's closed-loop gain is

$$|A_v| \cong \frac{R_F}{R_1} = \frac{10 \text{ k}\Omega}{1 \text{ k}\Omega} = 10.$$

Since the 1000 Hz is applied in a differential mode, it is amplified by this gain factor. Thus, at 1000 Hz, the output signal is

$$V_o \cong 10(10 \text{ mV}) = 100 \text{ mV}.$$

The 60-Hz noise voltage, on the other hand, is applied in common mode. Therefore, we first find the common-mode gain with Eq. (5-3); that is,

$$A_{cm} = \frac{A_v}{\text{CMRR}} \cong \frac{10}{10,000} = 1 \times 10^{-3},$$

where 80 dB is equal to the ratio 10,000.

We can find the amount of common-mode output voltage with Eq. (5-1); that is,

$$V_{cmo} = A_{cm}V_{cm} \cong 1 \times 10^{-3}(10 \text{ mV}) = 10 \text{ } \mu\text{V}.$$

Thus, the 60-Hz output is smaller than the input induced 60 Hz, by the factor 1000, and the Op Amp's differential input is effective in reducing noise problems. V_{cmo} can be in phase with V_{cm} as often as out of phase.

We could have determined the common-mode output V_{cmo} by using Eq. (5-5). For example, since a closed-loop gain of 10 is equivalent to 20 dB, then by Eq. (5-5b),

$$A_{cm} \text{ (dB)} = 20 - 80 = -60 \text{ dB}.$$

The negative sign means that the common-mode voltage is attenuated by 60 dB; that is, V_{cmo} is smaller than V_{cm} by the factor 1000.

5.3 MAXIMUM COMMON-MODE INPUT VOLTAGES

A common-mode input voltage can be dc as in the circuit of Fig. 5-5. In this case, the bridge circuit has one dc supply voltage E. By the voltage divider action of resistances R, a portion of this supply E is applied to inputs I and II. The dc voltages at these inputs are shown as V_1 and V_{II}. Their average value is the dc common-mode in put; that is,

$$V_{cm} = \frac{V_1 + V_{II}}{2}. \tag{5-6}$$

Further voltage-divider action takes place by resistors R_a and R_b, and by resistors R_1 and R_F, and the actual voltage applied to the noninverting input 2 is

$$V_2 = \frac{V_{II} R_b}{R_a + R_b}. \tag{5-7}$$

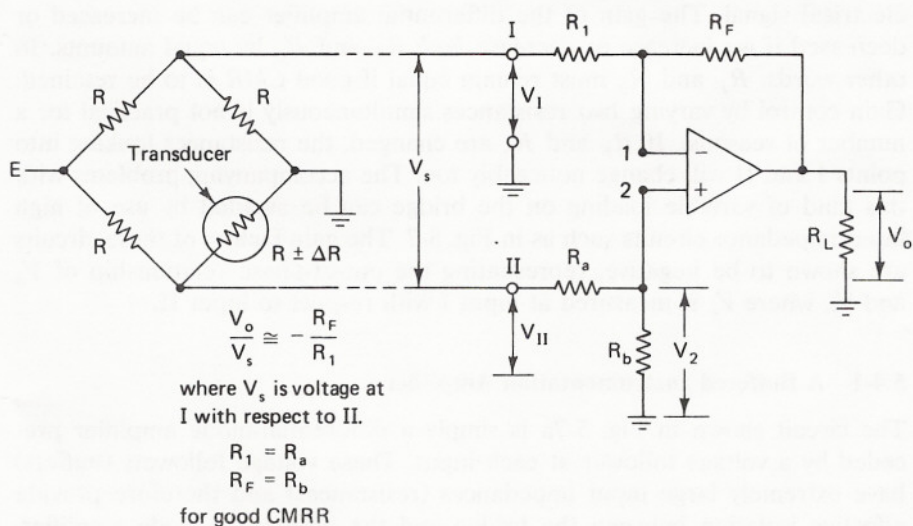Since V_1 is *virtually* at th same potential as V_2, then we can similarly show

$$\frac{V_o}{V_s} \cong -\frac{R_F}{R_1}$$

where V_s is voltage at I with respect to II.

$$R_1 = R_a$$
$$R_F = R_b$$

for good CMRR

Figure 5-5 Differential-mode circuit with a dc common-mode input.

that

$$V_1 \cong \frac{V_{\text{II}} R_b}{R_a + R_b}. \tag{5-8}$$

The voltage V_1 or V_2 should never exceed the maximum *input voltage* or the maximum *common-mode voltage* specified on an Op Amp's data sheets.
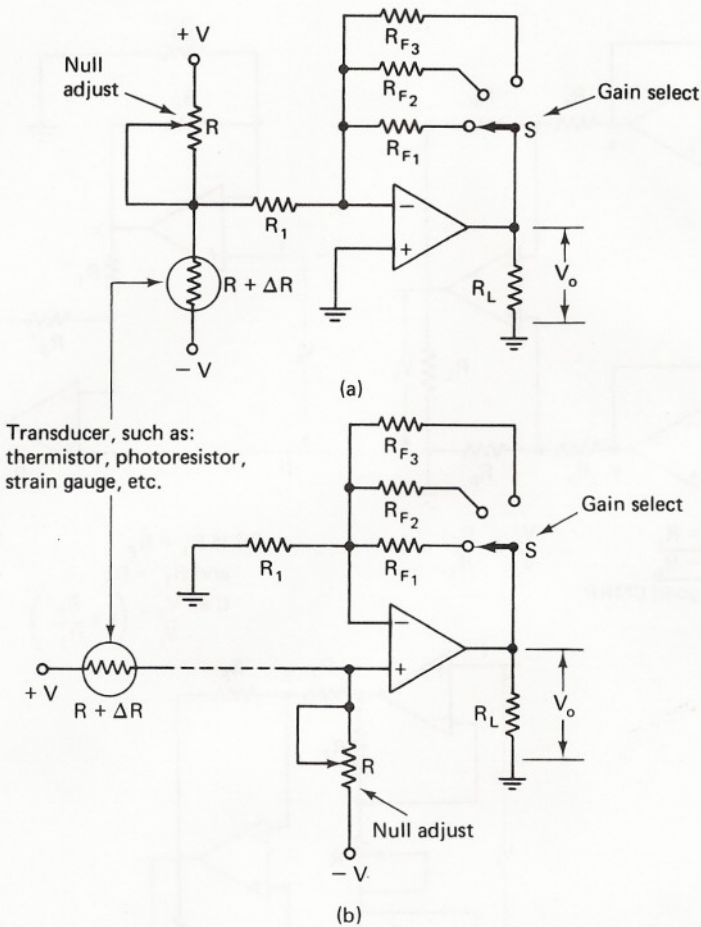
5.4   OP AMP INSTRUMENTATION CIRCUITS

Frequently, in instrumentation and industrial applications, the Op Amp is used to amplify signal output voltages from bridge circuits. We considered such a circuit earlier in Fig. 3-17a. Similar circuits are the useful *half-bridge* circuits as shown in Fig. 5-6. Because the inputs of these circuits are referenced to ground, they are prone to induced noise problems. Therefore, if the bridge-type transducer circuit is required to work in time-varying electric and magnetic fields, its amplifier should be a differential type, such as in Fig. 5-5.

In the circuit of Fig. 5-5, the maximum specified common-mode input voltage of the Op Amp dictates the maximum allowable dc source voltage E on the bridge. The transducer's resistance changes by ΔR when the appropriate change in its physical environment occurs. The bridge converts this physical change to a voltage change across points I and II which is amplified by the Op Amp. Thus, depending on the type of transducer used, a change in temperature, light intensity, strain, or whatever, is converted to an amplified electrical signal. The gain of the differential amplifier can be increased or decreased if we increase or decrease *both* R_F and R_b by equal amounts. In other words, R_F and R_b must remain equal if good *CMR* is to be retained. Gain control by varying *two* resistances simultaneously is not practical for a number of reasons.. If R_F and R_b are changed, the resistances looking into points I and II will change noticeably too. The accompanying problems with this kind of variable loading on the bridge can be avoided by use of high input impedance circuits such as in Fig. 5-7. The gain factors of these circuits are shown to be negative, representing the out-of-phase relationship of V_o and V_s, where V_s is measured at input I with respect to input II.

5.4-1   A Buffered Instrumentation Amplifier

The circuit shown in Fig. 5-7a is simply a differential-mode amplifier preceded by a voltage follower at each input. These voltage followers (buffers) have extremely large input impedances (resistances) and therefore provide effective isolation between the bridge and the differential-mode amplifier. Since each voltage follower's gain $A_v = 1$, the gain of the entire circuit is the

Figure 5-6 Half-bridge working into (a) an inverting circuit and (b) a noninverting circuit.

gain of the output differential stage. Thus, for the circuit shown in Fig. 5-7a,

$$\frac{V_o}{V_s} \cong \frac{R_F}{R_1}. \tag{3-4}$$

5.4-2 A Two-Op Amp Instrumentation Amplifier

The circuit in Fig. 5-7b also has high input impedance due to a noninverting-mode amplifier at each input. This circuit's differential gain V_o/V_s is deter-
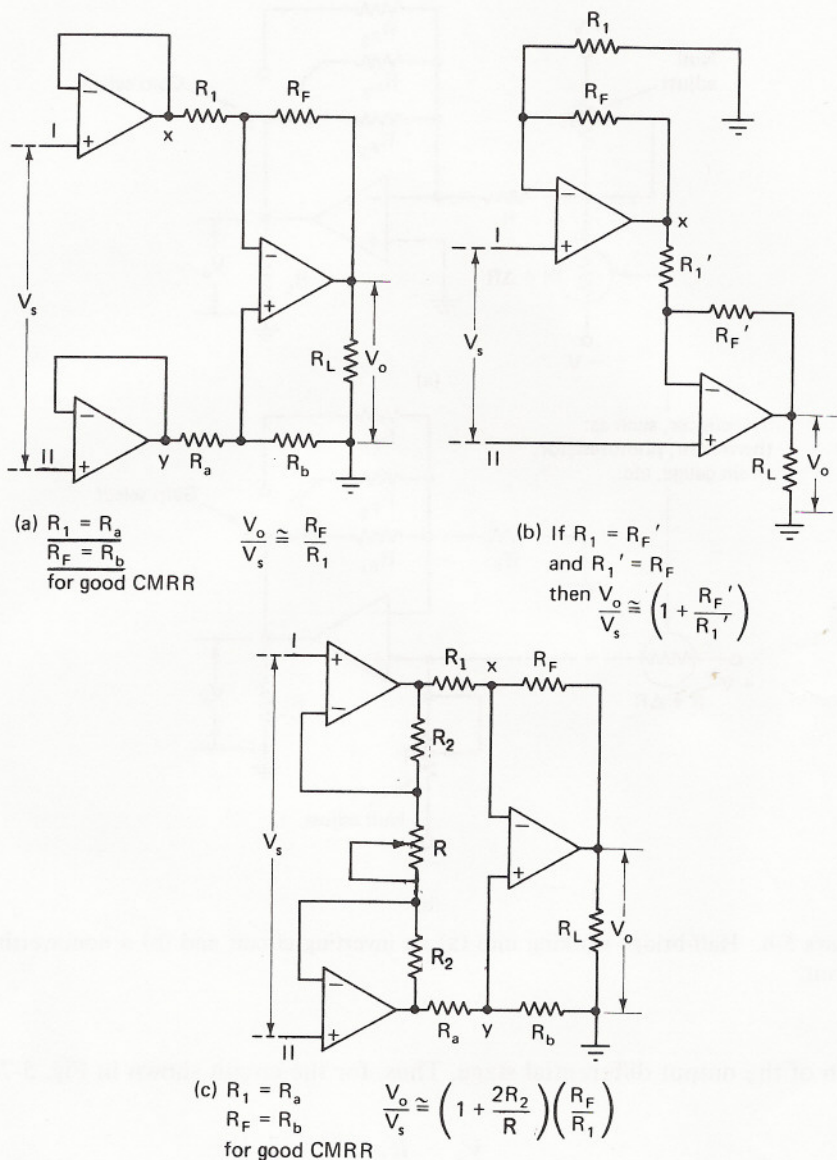
(a) $R_1 = R_a$
$R_F = R_b$
for good CMRR
$\dfrac{V_o}{V_s} \cong \dfrac{R_F}{R_1}$

(b) If $R_1 = R_F'$
and $R_1' = R_F$
then $\dfrac{V_o}{V_s} \cong \left(1 + \dfrac{R_F'}{R_1'}\right)$

(c) $R_1 = R_a$
$R_F = R_b$
for good CMRR
$\dfrac{V_o}{V_s} \cong \left(1 + \dfrac{2R_2}{R}\right)\left(\dfrac{R_F}{R_1}\right)$

Figure 5-7   High input impedance differential-mode amplifiers.

mined by the components connected on the output (lower) Op Amp; that is

$$\boxed{\dfrac{V_o}{V_s} \cong \left(1 + \dfrac{R_F'}{R_1'}\right).} \tag{5-9}$$

These voltage gains are negative (inverting) if V_s is referenced at input I with

respect to input II. Once the gain and components R'_1 and R'_F are selected; the components in the upper stage must comply with the equations

$$R_F = R'_1$$

and

$$R_1 = R'_F.$$

5.4-3 Variable Gain Instrumentation Amplifier

A useful instrumentation amplifier is shown in Fig. 5-7c. It has high input resistance, a good CMRR, and variable gain that is adjustable with the potentiometer R. Generally, smaller values of R provide larger gains. The equation for gain is easy to derive. Note in Fig. 5-8 that because $V_{id} \cong 0$ on both buffers, the input signal V_s must appear across the potentiometer R. Also we note that the output signal V_{o_1} of these buffers is across both resistors R_2 and the potentiometer R. These carry the same current and can be viewed as series resistors. By Ohm's law, then,

$$\frac{V_o}{V_s} = \frac{(R_2 + R + R_2)I}{RI} = \frac{(2R_2 + R)I}{RI},$$

where I is the signal current that cancels to show that these buffers have a gain of

$$\frac{V_{o_1}}{V_s} = \frac{(2R_2 + R)}{R} = \frac{2R_2}{R} + 1.$$

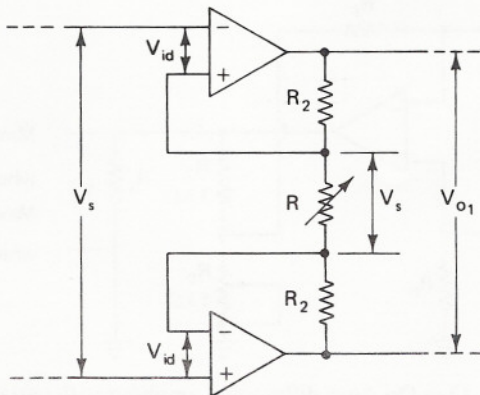The differential stage, following the buffers, has a gain of R_F/R_1. This,

Figure 5-8 Buffer stage for instrumentation amplifier has variable gain.

combined with the gain of the buffers, yields a total gain of

$$\frac{V_o}{V_s} \cong \left(1 + \frac{2R_2}{R}\right)\left(\frac{R_F}{R_1}\right). \qquad (5\text{-}10)$$

5.4-4 Simple One-Op Amp Instrumentation Amplifier

Another variable-gain differential-mode amplifier is shown in Fig. 5-9. Its gain V_o/V_s is varied by an adjustment of the potentiometer R_3, though its CMRR is affected thereby. Generally, the gain is increased or decreased by a decrease or increase of R_3, respectively. In this circuit, the right end of the feedback resistor R_F is connected to a voltage divider and the output signal voltage V_o is across this divider. When R_3 is maximum, half as much signal is fed back to the inverting input via R_F than would be the case if R_F were connected directly to the output as in the simpler differential amplifier in Fig. 5-3a. Thus the minimum gain can be estimated with the equation:

$$\frac{V_o}{V_s} \cong 2\left(\frac{R_F}{R_1}\right). \qquad (5\text{-}11)$$

This shows that twice as much gain occurs with half as much negative feedback. If R_3 is adjusted to a minimum of 0 Ω, the right end of R_F is grounded and no negative feedback occurs. This pulls the stage gain up to
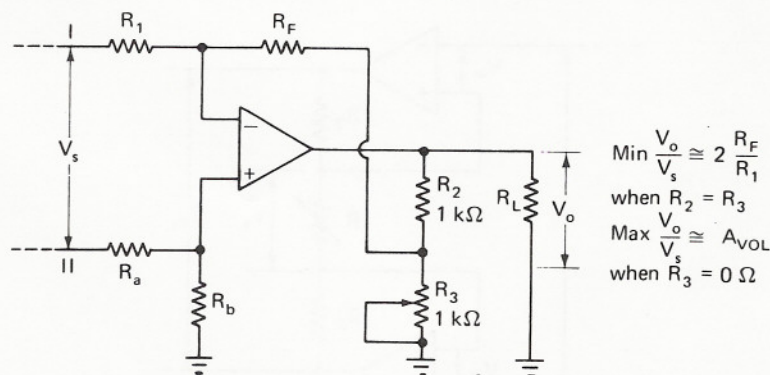

Figure 5-9 One Op Amp differential amplifier with variable gain.

the open-loop gain A_{VOL} of the Op Amp. Of course, both inputs can be preceded with voltage followers if high input impedance is required.